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4	US 5630105 A		USPAT	19970513	78
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(54) **INTERFACE CIRCUIT**

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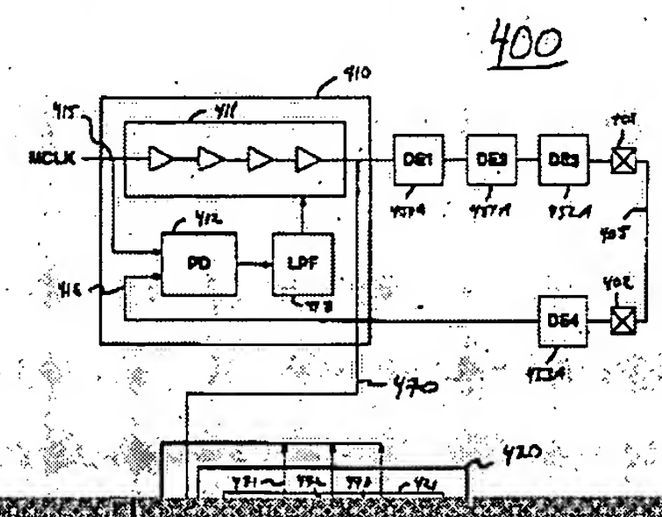
(57) **ABSTRACT**

An interface circuit according to one embodiment of the present invention includes a clock signal, a first phase locked loop coupled to the clock signal line and generating a reference clock signal, a second phase locked loop receiving the reference clock signal, and in accordance therewith, generating one or more phase shifted reference clock signals, and a data transceiver circuit coupled to receive at least one of the clock signal, the reference clock signal, or one or more of the phase shifted reference clock signals to control the flow of data between a first circuit and a second circuit. An interface circuit according to one embodiment of the invention can be used advantageously for controlling the flow of data between a CPU and an external memory.



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